A CMOS image sensor working as high-speed photo receivers as well as a position sensor for indoor optical wireless LAN systems


*Graduate School of Materials Science, Nara Institute of Science and Technology, 8916-5 Takayama, Ikoma 630-0101 JAPAN
**MICROSIGNAL Co., LTD, 1-7 Hikaridai, Seika, Souraku 619-0237 JAPAN

ABSTRACT

We propose and demonstrate a new image sensor specialized in an optical wireless LAN (local area network) system. The use of the image sensor brings excellent features to the optical wireless LAN systems; because the image sensor can capture the scene around the communication node or the hub at once like ordinary image sensors, it is easy to implement detection and tracing of the nodes or the hub without any mechanical component to search them. In addition, the image sensors inherently catch the multiple optical signals in parallel by a huge amount of micro photodiodes, which means that they have potentiality of concurrent data acquisition from multiple nodes at the hub. In this paper, we describe a pixel structure to implement two functional modes: a communication (COM) mode to receive temporally modulated optical signals and an image sensor (IS) mode to capture an image in which photodiode operates in an integration mode. The pixel is a fusion of an active pixel sensor and a current amplifier without temporal integration. We fabricated an 8x8-pixel image sensor in a standard 0.8μm BiCMOS technology, and successfully demonstrated position detection of a light source and acquisition of optical serial data when wavelength and frequency of incident optical data were 830nm and 1MHz, respectively. We also show the design of a 50x50-pixel CMOS image sensor with 3-stage main amplifiers.

Keywords: optical wireless LAN, CMOS image sensor, free-space optical interconnection.

1. INTRODUCTION

An indoor optical wireless LAN (Fig. 1) is one of the promising options to realize ultra wide band wireless communication due to the following advantages over the other LAN regimes by an electric wire, an optical fiber, and a radio frequency electromagnetic wave: small investment required in introduction, potentiality of broadband communication at the speed of over GHz demonstrated in optical fiber communications, little interference with electronic equipments, and security. Several indoor optical wireless LAN systems are now commercially available [1].

We propose a new scheme of indoor optical wireless LAN, in which a CMOS image sensor (CIS) is utilized as a photoreceiver as well as a two-dimensional position-sensing device for detecting the positions of communication modules of nodes or a hub, while a single or at most several photodiodes are utilized to receive optical signals in the conventional systems. Figure 2 compares our scheme of indoor optical wireless LAN system with the conventional one. In the optical wireless LAN, optical signals should be transmitted toward the counterpart accurately to obtain enough optical input power incident on the photodetector. Therefore, position detection of the communication modules and alignment of the light are significant. In a conventional optical wireless LAN system with a function of automatic node detection and targeting, as shown in Fig. 2(a), a mechanical scanning system of the photodetection optics is implemented for searching the hub at the node. However, the volume of the scanning system becomes bulky because the diameter of the focusing lens should be large to gather enough optical power.

E-mail: kagawa@ms.aist-nara.ac.jp
On the other hand, as shown in Fig. 2(b), we propose to use an image sensor as a photoreceiver. This approach brings excellent features to the optical wireless LAN systems; because an image sensor can capture the surroundings around the communication module at once, it is easy to specify the positions of the other modules by use of simple image recognition algorithms without any mechanical component. Another feature is concurrent communication. Image sensors inherently catch the multiple optical signals in parallel by a huge number of micro photodiodes, and the different modules are detected by the independent pixels when the image sensor has enough spatial resolution. These facts imply potentiality of space division multiple access (SDMA). SDMA brings several advantages over time, code or frequency division multiple accesses (TDMA, CDMA, or FDMA). Our approach is also effective for high-speed operation of photodiodes. Response time of the photodiode is mainly determined by its parasitic capacitance, which is almost proportional to the area of the photodiode.

In spite of the above advantages, it is difficult to directly apply the image sensor to the optical wireless LAN systems because they cannot detect high-speed signals modulated in time domain. The existing image sensors integrate photocurrents for sub milli to several seconds to realize high photosensitivity. In addition, the image is read out pixel by pixel by scanning. In this paper, we propose and preliminarily demonstrate a CIS specialized in the optical wireless LAN, which has two functional modes: IS (image sensor) and COM (communication) modes.

2. INDOOR OPTICAL WIRELESS LAN SYSTEM USING A CMOS IMAGE SENSOR

The proposed CIS has two functional modes: an image sensor (IS) mode and a communication (COM) mode. In the IS mode, the CIS obtains an image of the surroundings like ordinary image sensors. On the other hand, in the COM mode, photocurrents are directly read out without temporal integration from the specific pixels receiving optical signals as shown in Fig. 3. Optical signals from the different communication modules are read out in parallel through the independent signal lines. To read out the photocurrent in the COM mode, what we call a focused readout is utilized.

Fig. 2. (a) Conventional and (b) our configurations.

Fig. 3. (a) Focused readout of multiple optical signals and (b) schematic of focused readout on the CIS.
shown in Fig. 3(b), a light signal from a communication module is received by one to a few pixels, because the focused light spot has finite size. In the COM mode, the amplified photocurrents from the pixels receiving the optical signals are summed up to the same readout line prepared for the COM mode, so that the signal level does not reduce. If we prepare multiple readout lines, SDMA becomes possible. When optical signals from the different communication modules are received by the independent pixels and read out to the separate readout lines, concurrent data acquisition from multiple modules can be achieved. Consequently, we can increase the total bandwidth of the uplink in proportion to the number of the readout lines. When the readout line is in conflict among multiple nodes, TDMA is used with SDMA. In this case, the hub gives short time slots to each node in turn to share the readout line.

Figure 4 shows a procedure to establish a data link between a node and a hub. The procedure consists of two stages: a stage of position detection and a communication stage. In the procedure, a wide-angle diffusive light and a narrow collimated light beam are complementally used. At first, the hub and the node do not know existence of the other. Figure 4(a) depicts a stage of position detection. Both hub and node work in the IS mode. They transmit the diffusive light to notify their existence to the other. To cover the large area where the counterpart possibly exists, diffusive light with wide radiation angle $2\Theta$ is utilized. Because the optical power detected at the counterpart is generally very weak, it is effective to detect it in the IS mode. It is widely known that we can achieve outstandingly high conversion gain (output voltage/photocurrent) at extremely low power consumption with the integration mode of photodiode, which is utilized in almost all image sensors. To distinguish the notification light from illumination lights such as a fluorescent light, the light intensity is modulated with a specific temporal pattern, for example, an alternative binary pattern with frequency of several hertz. The light spot from the counterpart in the captured image is detected by use of a digital signal processor connected to the CIS.

After the positions are specified, we proceed to the next stage. The functional mode of the CIS for both the node and the hub is switched to the COM mode. As shown in Fig. 4(b), they emit a narrow collimated beam carrying communication data in the detected position toward the counterpart. The hub and the nodes have unique ID’s corresponding to MAC addresses in Ethernet to identify sources and destinations of communication. At the hub, the detected nodes are added to the communication list after data path is established. To find the new communication modules, the procedure for detecting the nodes is executed concurrently with the other procedures. On the other hand, at the node, it is enough to catch position of the hub alone. When signal level from the counterpart becomes less than predefined threshold level due to movement or shutdown of the communication modules, it is eliminated from the communication list. With intelligent algorithms to trace relative movement of the counterpart, optical communication is not interrupted.

3. STRUCTURE OF THE CMOS IMAGE SENSOR

The special image sensor for the optical wireless LAN can be fabricated by a standard CMOS technology. Unlike CCD image sensors widely used in digital still cameras and video cameras, various processing circuits such as photoamplifiers and logic circuits can be integrated with photodiodes. Figure 5 shows the structure of the fundamental pixel circuit of the proposed CIS. By configuring switches S1, S2, and S3, the pixel works as an active pixel sensor (APS)[2, 3] and a photodiode with a current amplifier, which are for the IS and COM modes, respectively. APS is a fundamental component of the CIS’s, and offers high photosensitivity because it temporally integrates photocurrents. When S1 and S3 are OFF and S2 is ON, the anode of the photodiode is connected to the ground, and this circuit works as an APS, in which photocurrent is temporally integrated at the junction capacitor of the photodiode. The pixel value is read out to IS_OUT. On the other hand, when S1 and S3 are ON and S2 is OFF, the cathode of the photodiode is reverse-biased to the power supply voltage VDD, and photocurrent is read out to COM_OUT without temporal integration after amplified
by the current amplifier. Switch S3 is prepared for minimizing the power consumption. Only when the pixel receives
the light signal, S3 should be ON and the in-pixel amplifier works. In our CIS, almost all pixels work in the IS mode
because the number of pixels receiving optical signals is as many as a few multiplied by the number of the communica-
tion modules. Therefore, S3 greatly contributes to low power consumption.

Figure 6 shows an example of the pixel circuit with two independent high-speed readout lines. For the focused read-
out, digital elements such as memories and a functional mode decoder are added to the circuit shown in Fig. 5. D-
latches memorize selection of the COM_OUT lines. When XS and YS are high at the same time (that means the pixel
is selected), DAT#1 and #2 are written in the D-latches. The NOR gate decodes the functional mode from the contents
of D-latches. When one of the D-latches is high, the NOR puts out low and the pixel works in the COM mode. Oth-
nerwise, the output of the NOR is high, and the pixel works in the IS mode. Note that the case that DAT#1 and #2 are
high at the same time is forbidden.

4. DESIGN AND EXPERIMENTAL RESULTS

To demonstrate the fundamental operations of the proposed CIS, we fabricated an 8x8-pixel CIS by use of a standard 0.8
µm BiCMOS technology. The BiCMOS technology enables us to fabricate high-speed photodiodes by use of a buried
collector layer for a bipolar transistor because slow diffusive carriers generated in the substrate is blocked by the buried
collector layer [4, 5]. The pixel circuit was the same as Fig. 6. W/L of the transistors was 2.0 µm/ 0.8 µm, and the in-
pixel photocurrent amplifier was omitted for simplicity. The layout of the pixel and the photograph of the CIS are
shown in Figs. 7 (a) and (b), respectively. The pixel size and fill factor are 160 µm sq. and 14%, respectively. For I-
V conversion of the photocurrent in the COM mode, a transimpedance amplifier with transimpedance gain of 2 kΩ was
used [6]. Figure 8 shows the experimental results of the CIS. In the experiments, a pulse-modulated laser beam
whose wavelength and frequency were 830 nm and 1 MHz, respectively, was focused on the center pixel of the CIS.
VDD was 5.0 V. Fig. 8(a) is an oscilloscope trace in the IS mode, in which all the pixels are read out by scanning
along every row except the row #8. The optical power and integration time were 1.1 nW and 29.6 ms, respectively,
which meant that image capturing at the video rate was possible. Then, the functional mode of the center pixel was
changed to the IS mode. As shown in Fig. 11(b), the eye pattern was successfully obtained from the center pixel when
the optical power was 519 µW. Photosensitivity was 0.06 A/W.
Fig. 7. (a) Pixel layout and (b) microphotography of the CIS.

Fig. 8. (a) Output waveform in the IS mode and (b) eye diagram in the COM mode.

Fig. 9. (a) Schematic of the pixel with an in-pixel amplifier and (b) frequency response.
Although the BiCMOS technology enables us to fabricate high-speed photodiodes by use of a buried collector layer for a bipolar transistor, the bit rate is slow in the above experiments. The main reason is large time constant caused by parasitic capacitors and resistors accompanying the readout lines and the photodiode because the pixel does not have in-pixel photocurrent amplifier. To verify effectiveness of the in-pixel current amplifier, we designed a test pixel circuit with in-pixel current amplifier shown in Fig. 9(a). The pixel works in the COM mode when MODE_SELECT is low. The photocurrent is firstly amplified by the current-voltage converter composed of two NPN bipolar transistors, a diode-connected bipolar transistor, and two current loads (M1 and M2). The amplified voltage signal is converted to current again by the transistor M3. The output current COM_OUT is measured by an oscilloscope after converted to the voltage signal by an off-chip amplifier. Figure 9(b) shows the frequency response of the test pixel circuit. VDD was 5.0 V. Operation speed up to 100 MHz was verified. The current gain was about 6.

To increase the number of pixels, we have designed the CIS in a standard 0.35 µm CMOS technology by use of HSPICE. Figure 10 and 11 show schematic diagram of the whole chip and pixel layout, respectively. Figure 12 shows the schematic of the whole circuit. Each pixel has a transimpedance amplifier to amplify photocurrent. High-speed readout lines are prepared for each column, and each line is shared by pixels of neighboring two columns. A main amplifier is prepared for each column, which is composed of three amplifiers. The first amplifier converts the output current from the pixels, and the voltage signal is amplified by following two differential amplifiers. Four of the
outputs from the column amplifiers can be read out to off chip through the multiplexer. The differential pair of the output signals is accompanied with the bias current to cancel the offset current of the in-pixel amplifier (about 100 µA), and the signal to control the gain of the main amplifier. By use of these signals, we can realize automatic gain control and automatic offset cancel. The specifications are summarized in Table 1.

<table>
<thead>
<tr>
<th>Chip size</th>
<th>4.9 mm sq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of pixels</td>
<td>50 x 50</td>
</tr>
<tr>
<td>Pixel size</td>
<td>60 µm sq.</td>
</tr>
<tr>
<td>Fill factor</td>
<td>16%</td>
</tr>
<tr>
<td>Bandwidth @-3dB</td>
<td>213 MHz</td>
</tr>
<tr>
<td>Slew rate</td>
<td>170 V/µs</td>
</tr>
<tr>
<td>Current gain of in-pixel amplifier</td>
<td>17</td>
</tr>
<tr>
<td>Transimpedance gain</td>
<td>206 kΩ</td>
</tr>
<tr>
<td>Cross-talk between two high-speed readout lines</td>
<td>-67dB</td>
</tr>
</tbody>
</table>

5. FUTURE ISSUES

Data transfer rate of the proposed system is a great concern. The maximum speed of our CIS is mainly limited by the maximum operational frequency of a photodiode, which is realized as a parasitic device in a standard VLSI technology. Although the photodiode is not optimized in terms of dark current, photosensitivity, operational speed, and so on, it is possible to fabricate silicon monolithic photoreceivers with operational speed of more than 1 GHz by use of standard BiCMOS technologies. In addition, fast photoreceivers by use of standard CMOS or CMOS SOI (silicon on insulator) technologies are also reported [7-9]. Judging from the results of these former works, we are convinced that data transfer rate more than 1Gbps is achievable.

Design of an in-pixel amplifier is a significant issue. We should care about trade-off between circuit area, gain and speed, saturation of the amplifier, and layout minimizing cross-talk. The in-pixel amplifier should be small but fast. When we consider noise during signal transmission to the main amplifier outside the pixel array, gain of the in-pixel amplifier should large. However, the gain is limited by the circuit area. In our opinion, we should respect operational speed rather than gain, because large gain can be achieved by the main amplifier outside the array where large circuit area is available. Another point of design is saturation level of the amplifier for optical input power. Unlike optical fiber communication, lights from various light sources except the communication modules, such as fluorescent lights and LED indicators, are incident on the photoreceiver. Therefore, offset photocurrent generated by the illuminations causes saturation of the amplifiers when the total gain of the amplifiers is large. To avoid the problem, circuits that cancel the offset current are necessary. In addition, cross-talk between pixels should be considered in layout, because scanners for reading out the image and in-pixel digital circuits work while the optical signals are read out. Analog circuits and photodiodes should be separated from the digital signal lines and circuits generating noises. We also consider noise of amplifiers in designing circuits and evaluate bit error rate by both simulation and experiments.

6. CONCLUSIONS

We proposed a new scheme of indoor optical wireless LAN systems based on a special CMOS image sensor (CIS) enabling a compact and low-power communication module with large capacity of uplink. The CIS has two functional modes: an image sensor mode and a communication mode for position detection and tracing of communication modules (of nodes and a hub) and free-space optical communication, respectively. To realize the CIS, a new pixel structure working as an active pixel sensor and a direct photocurrent amplifier without integration was proposed. To demonstrate the fundamental operations of the proposed CIS, an 8x8-pixel CIS was fabricated using a standard 0.8 µm BiCMOS technology. From the experimental results, the image and the eye pattern of the optical signals with frequency of 1 MHz incident on the center of the CIS were successfully obtained by selecting the functional modes. By the test pixel circuit with an in-pixel current amplifier, we verified that operation speed was improved to 100 MHz. A 50x50-pixel CIS for optical wireless LAN was designed in a standard 0.35µm CMOS technology. This chip is due to March, 2003.
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